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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/782,513 | 02/18/2004 | Alexander Burinskiy | 08211/0200373-US0/P05759 | 4709 |

38845 7590 07/28/2005

DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

| EXAMINER | |
|---|---|
| TRA, ANH QUAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/782,513 | BURINSKIY ET AL. | |
| | Examiner | Art Unit | |
| | Quan Tra | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-11,14 and 15* is/are allowed.

6)☒ Claim(s) *1-8,12,16-24 and 26* is/are rejected.

7)☒ Claim(s) *13 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to the amendment filed 06/21/05. The rejection in previous office action is maintained.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 6-8, 18-23 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Ichiki (JP 2001-185964).

As to claim 1, Ichiki discloses in figure 3B a current regulation circuit, comprising: a current mirror (201, 202p) arranged with a sense transistor (201p) and a power transistor (202p); a current sink that is coupled to a drain of the sense transistor (as shown), wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit; and a control component (the comparator) that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor.

As to claim 6, figure 3B shows that the control component senses a feedback signal provided by a load coupled to a drain of the power amplifier, wherein the feedback signal is employed in the control of the operation of the control component.

As to claim 7, figure 3B shows that the current mirror of the power transistor and the sense resistor employs a ratio of m:1.

As to claim 8, figure 3B shows that the sense transistor and the power transistor are at least field effect transistors (FET).

As to claim 18, figure 3B shows that the power transistor is an input-side transistor of the current mirror, and wherein the sense transistor is an output-side transistor of the current mirror.

As to claim 19, figure 3B shows that the sense transistor has at least a drain, the current mirror has at least an input and an output, and wherein the output of the current mirror is the drain of the sense transistor.

As to claim 20, figure 3B shows that the current sink is arranged such that, if the current flowing through the power transistor is less than a limit the current sink pulls down the drain voltage of the sense transistor such that the drain voltage of the sense transistor is less than the drain voltage of the power transistor (when current Iout is less that Iref, output of the amplifier is high, thereby turns off transistors 201 and 202. The current source then pulls down the voltage at the drain of transistor 201 to a voltage lower than the voltage at the drain of transistor 202).

As to claim 21, figure 3B shows that the control circuit is further arranged to control the power transistor such that voltage regulation is performed based on the control of the power transistor.

As to claim 22, figure 3B shows that the control circuit is arranged to virtually eliminate the channel modulation effect of the current mirror without invoking a special circuit to equalize the drain-to-source voltage of the sense transistor with the drain-to-source voltage of the power transistor.

As to claim 23, figure 3B shows that the control circuit includes a comparator that is arranged to trip if a drain-to-source voltage of the sense transistor reaches (crosses) a drain-to-source voltage of the power transistor, wherein the control circuit is further arranged to turn off the power and sense transistors if the comparator is tripped.

As to claim 26, figure aB shows a regulator circuit, comprising: a current mirror including an input-side transistor (202) and an output-side transistor (201); a current source that is coupled to a drain of the output-side transistor, wherein the current source pulls up a drain voltage of the output-side transistor if a current flowing through the input side transistor is less than a limit; and a control component (203) that is arranged to limit the current flowing through the input-side transistor if a drain-to-source voltage of the output-side transistor is substantially equivalent to a drain-to-source voltage of the input-side transistor.

3. Claims 1-8, 12, 16-23 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Magoon (USP 6744795).

As to claim 1, Magoon discloses in figure 4 a current regulation circuit (302, 305, 306, 312, 326). It is noted that column 4, lines 61-65, teaches that the transistors may be p-channel FETs. Therefore, the transistor types and polarities of the supply voltage in circuit 300 are reversed, such as shown in Shuzo's figure 3B cited above. Magoon's current regulation circuit comprising: a current mirror (p channel FETs 305 and 306) arranged with a sense transistor (305) and a power transistor (306); a current sink (302) that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit; and a control component (326) that is

arranged to limit the current flowing through the power transistor if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor.

As to claim 2, figure 4 further shows a component (312) that outputs a signal if the drain voltage of the sense resistor is substantially equivalent to the drain voltage of the power transistor.

As to claim 3, figure 4 shows that the component (312) is at least one of a comparator and a differential amplifier.

As to claim 4, figure 4 shows that the control component employs the signal to substantially turn off the current flowing through the power transistor.

As to claim 5, figure 4 shows that the control component employs the signal to modulate the amount of current flowing through the power transistor to be less than the limit.

As to claim 6, figure 4 shows that the control component senses a feedback signal provided by a load coupled to a drain of the power amplifier, wherein the feedback signal is employed in the control of the operation of the control component.

As to claim 7, figure 4 shows that the current mirror of the power transistor and the sense resistor employs a ratio of m:1.

As to claim 8, figure 4 shows that the sense transistor and the power transistor are at least field effect transistors (FET).

As to claim 12, figure 4 shows a current regulator, comprising a current mirror (p channel FETs 305 and 306) arranged with a sense transistor (305) and a power transistor (306), a current sink (302) that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a

limit; a control component (326) that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor; and a comparison component (312) that presents a signal if the drain voltage of the sense resistor is substantially equivalent to the drain voltage of the power transistor.

As to claim 16, figure 4 shows that the current flowing through the power transistor is substantially continuous.

As to claim 17, figure 4 shows a current regulation circuit, comprising a means (connection line) for mirroring current flowing in a sense transistor (305) and a power transistor (306), a means (302) for sinking current that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit; a means (326) for limiting the current flowing through the power transistor if the drain voltage of the sense transistor is substantially equivalent to a drain voltage of the power transistor; and a means (312) for presenting a signal if the drain voltage of the sense transistor is substantially equivalent to the drain voltage of the power transistor.

As to claim 18, figure 4 shows that the power transistor is an input-side transistor of the current mirror, and wherein the sense transistor is an output-side transistor of the current mirror.

As to claim 19, figure 4 shows that the sense transistor has at least a drain, the current mirror has at least an input and an output, and wherein the output of the current mirror is the drain of the sense transistor.

As to claim 20, figure 4 shows that the current sink is arranged such that, if the current

flowing through the power transistor is less than a limit the current sink pulls down the drain voltage of the sense transistor such that the drain voltage of the sense transistor is less than the drain voltage of the power transistor (when the output current is less that Iref, output of the amplifier is high, thereby turns off the PMOS transistors 305 and 306. The current source then pulls down the voltage at the drain of transistor 305 to a voltage lower than the voltage at the drain of transistor 206).

As to claim 21, figure 4 shows that the control circuit is further arranged to control the power transistor such that voltage regulation is performed based on the control of the power transistor.

As to claim 22, figure 4 shows that the control circuit is arranged to virtually eliminate the channel modulation effect of the current mirror without invoking a special circuit to equalize the drain-to-source voltage of the sense transistor with the drain-to-source voltage of the power transistor.

As to claim 23, figure 4 shows that the control circuit includes a comparator that is arranged to trip if a drain-to-source voltage of the sense transistor reaches (crosses) a drain-to-source voltage of the power transistor, wherein the control circuit is further arranged to turn off the power and sense transistors if the comparator is tripped.

As to claim 26, figure 4 shows a regulator circuit, comprising: a current mirror including an input-side transistor (306) and an output-side transistor (305); a current source (302) that is coupled to a drain of the output-side transistor, wherein the current source pulls up a drain voltage of the output-side transistor if a current flowing through the input side transistor is less than a limit; and a control component (312) that is arranged to limit the current flowing through

the input-side transistor if a drain-to-source voltage of the output-side transistor is substantially equivalent to a drain-to-source voltage of the input-side transistor.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ichiki (JP 2001-185964) or Magoon (USP 6744795).

The Ichiki or Magoon reference fails to teach that the power transistor has a m:1 ratio over the sense transistor, wherein m is greater than one. However, output transistor is greater than input transistor or vice versa in a current mirror circuit in order to generate a desired output current is well known in the art. Therefore, it would have been obvious to make the power transistor greater than the sense transistor for the purpose of providing a current greater than the sense current.

***Allowable Subject Matter***

6. Claims 13 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9-11, 14 and 15 are allowed.

Claim 25 would be allowable because the prior art fails to shows the detail of the feedback circuit as claimed.

***Response to Arguments***

7. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that the Ichiki does not disclose that the current sink pulls down a drain voltage of the sense transistor if a current flowing through the power transistor is less than a limit, as recited in Applicant's Claim 1. The Examiner respectfully disagrees. One skill in the art would have recognized that when the output current is less than the reference current, the voltage at the drain of transistor 202 is less than the voltage at the drain of transistor 201. Then, the comparator outputs a high level, thereby turns off transistors 201 and 202. Then the current source (Iref) pulls down the voltage at the drain of transistor 201 to less than the voltage at the drain of transistor 202. it is noted that if the voltage at the drain of transistor 201 is not pulled lower than the voltage at the drain of transistor 202, the comparator can not provide a low signal in order to regulate the output voltage and current.

Applicant further argues that Ichiki does not disclose "a control component that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense transistor is substantially equivalent to a drain voltage of the power transistor". The Examiner respectfully disagrees. The comparator controls transistors 201 and 202 in order to maintain the voltages at the drains of the transistor to be substantially equal. The transistors are not fully on when the voltage at the drains of the transistors are equal. Thus, the currents that flowing through the transistor are limited by the comparator.

Applicant also states the same arguments for 102 rejection anticipated by Magoon reference. Magoon's figure 4 shows a circuit having NFETs and pull up current source (302). Magoon further teaches that the transistors may be PFET. It is inherent that the polarities of the

power supplies will be reversed if the transistor types are reversed. Therefore, if the transistors are pFETs, the current source 302 will function as a pull down current source. Magoon's figure 4 will have a similar structure as Ichiki's figure 3b. Therefore, the circuit will operates as discussed above.

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

July 26, 2005